IXYS

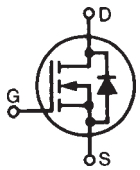
PolarHV™ HiPerFET Power MOSFET

IXFR 64N60P

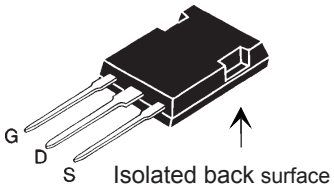
V_{DSS} = 600 V
I_{D25} = 36 A
$R_{DS(on)}$ ≤ 105 mΩ
t_{rr} ≤ 200 ns

(Electrically Isolated Back Surface)

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25° C to 150° C	600	V
V_{DGR}	T_J = 25° C to 150° C; R_{GS} = 1 MΩ	600	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	T_C = 25° C	36	A
I_{DM}	T_C = 25° C, pulse width limited by T_{JM}	150	A
I_{AR}	T_C = 25° C	64	A
E_{AR}	T_C = 25° C	80	mJ
E_{AS}	T_C = 25° C	3.5	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤100 A/μs, $V_{DD} \le V_{DSS}$, T_J ≤150° C, R_G = 2 Ω	20	V/ns
P_D	T_C = 25° C	360	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
F_C	Mounting force	22..130/5..29	N/lb
Weight	ISOPLUS247	5	g

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 3 mA	600			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8 mA	3.0		5.0	V
I_{GSS}	V_{GS} = ± 30 V_{DC}, V_{DS} = 0			± 200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			25	μA
	T_J = 125° C			1000	μA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$, Note 1			105	mΩ

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- International standard packages
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 20 V; I_D = I_T, Note 1	40	63		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		12		nF
C_{oss}			1150		pF
C_{rss}			80		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = I_T R_G = 1 Ω (External)		28		ns
t_r			23		ns
$t_{d(off)}$			79		ns
t_f			24		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = I_T		200		nC
Q_{gs}			70		nC
Q_{gd}			68		nC
R_{thJC}				0.35	°C/W
R_{thC}			0.15		°C/W

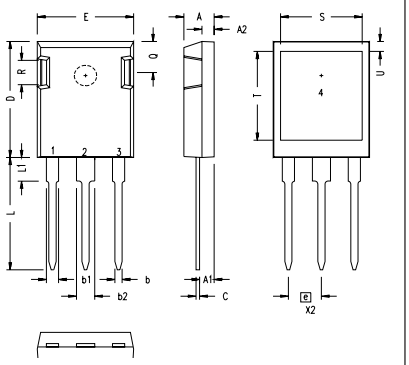
Source-Drain Diode

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			64	A
I_{SM}	Repetitive			150	A
V_{SD}	I_F = I_S, V_{GS} = 0 V,			1.5	V
t_{rr}	I_F = 25A, -di/dt = 100 A/μs			200	ns
Q_{RM}	V_R = 100V		0.6		μC
I_{RM}			6.0		A

Notes:

1. Pulse test, t ≤300 μs, duty cycle d ≤ 2 %;
2. Test current I_T = 32A.

ISOPLUS247 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Fig. 1. Output Characteristics @ 25ºC

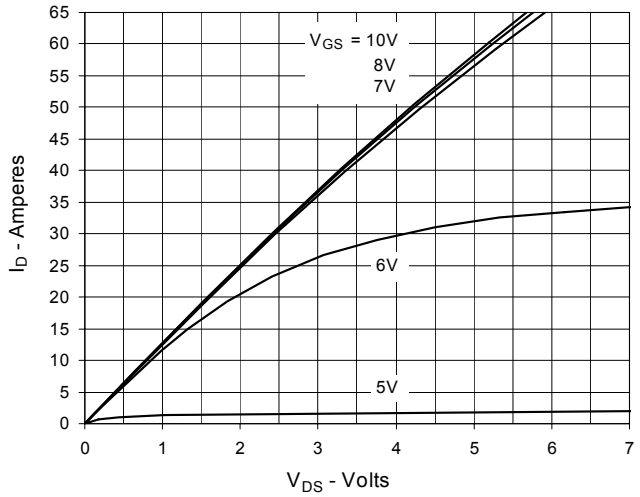


Fig. 2. Extended Output Characteristics @ 25ºC

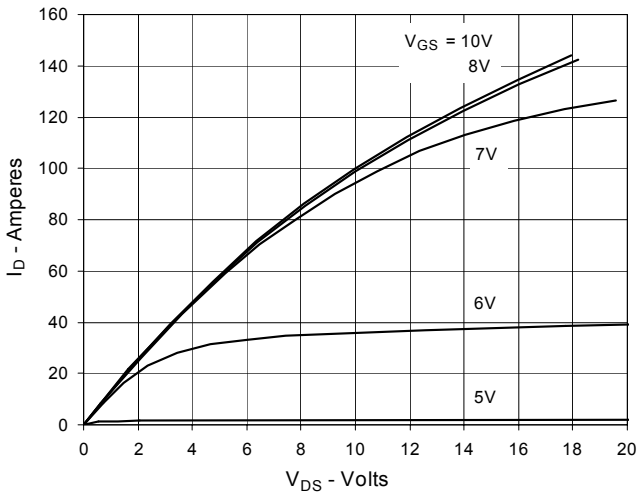


Fig. 3. Output Characteristics @ 125ºC

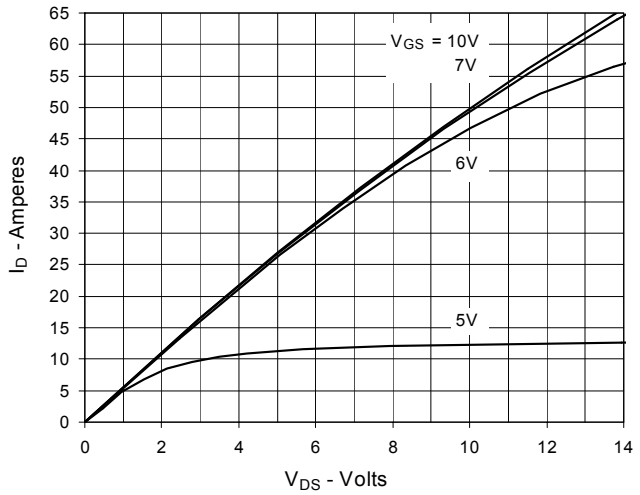


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 32A vs. Junction Temperature

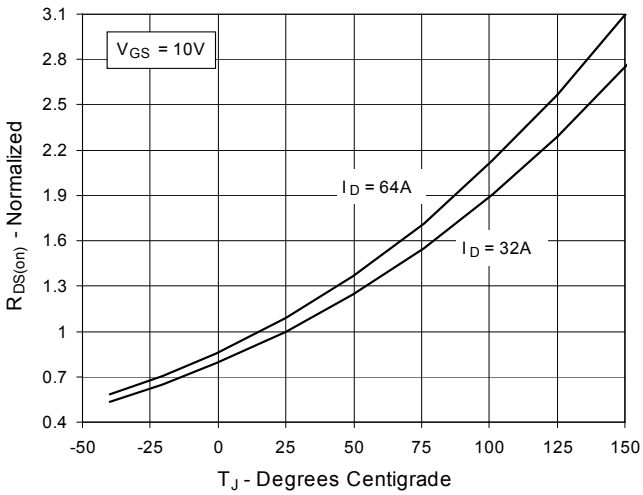


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 32A vs. Drain Current

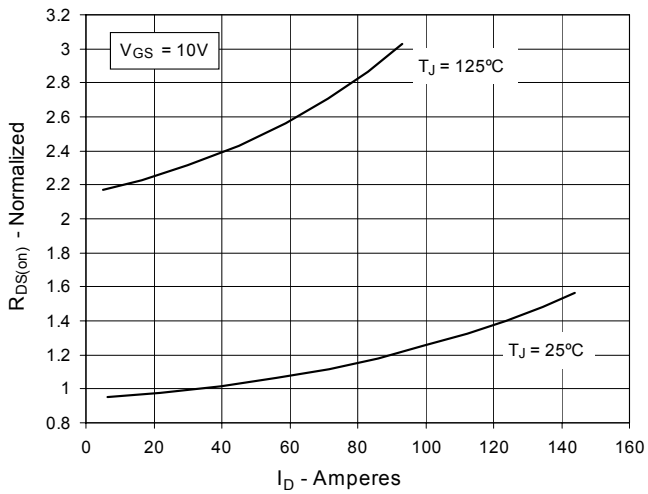


Fig. 6. Maximum Drain Current vs. Case Temperature

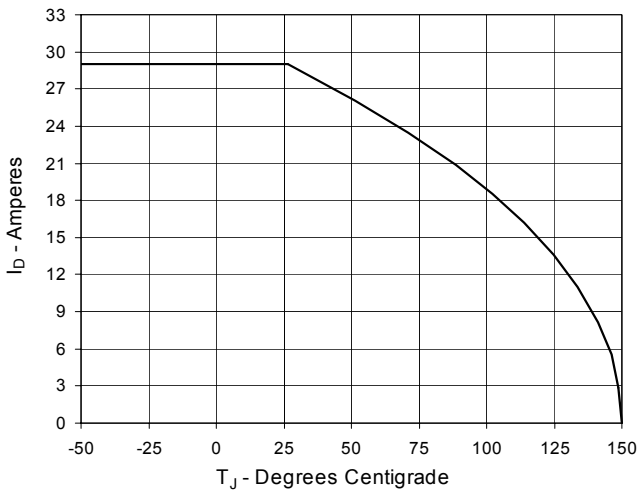


Fig. 7. Input Admittance

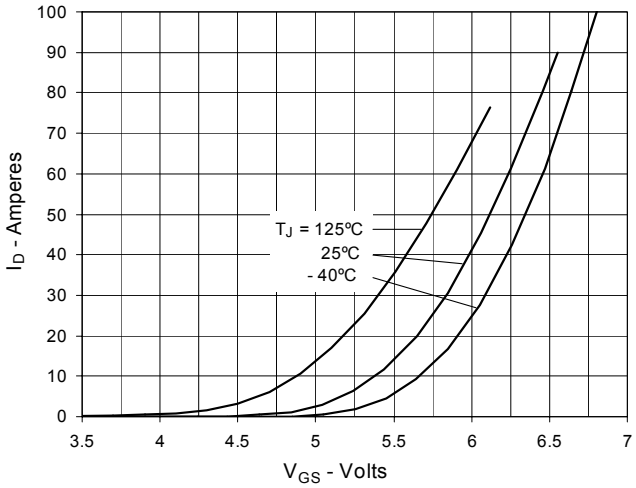


Fig. 8. Transconductance

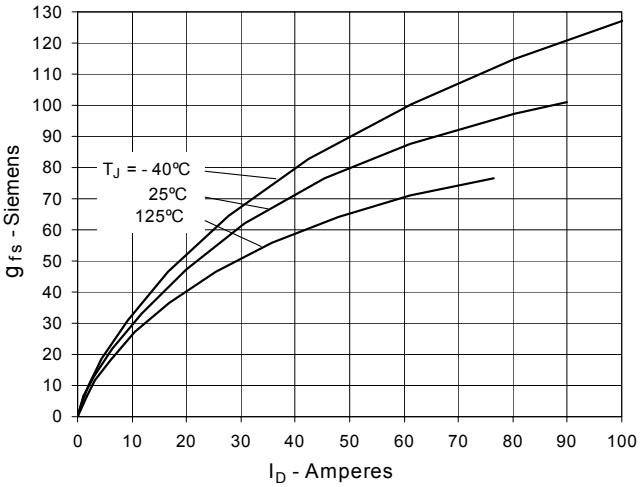


Fig. 9. Forward Voltage Drop of Intrinsic Diode

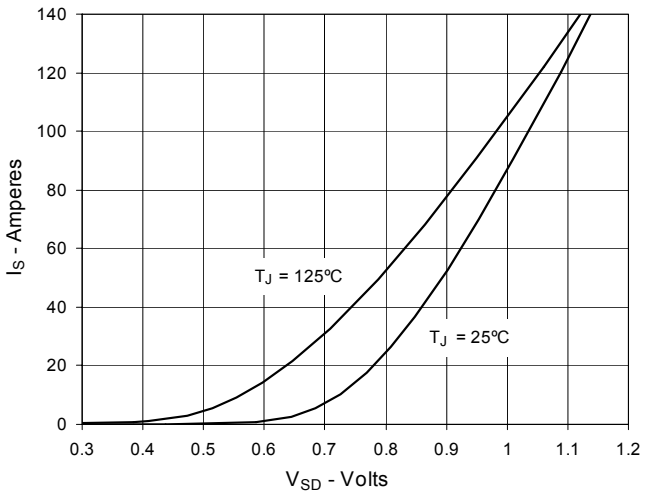


Fig. 10. Gate Charge

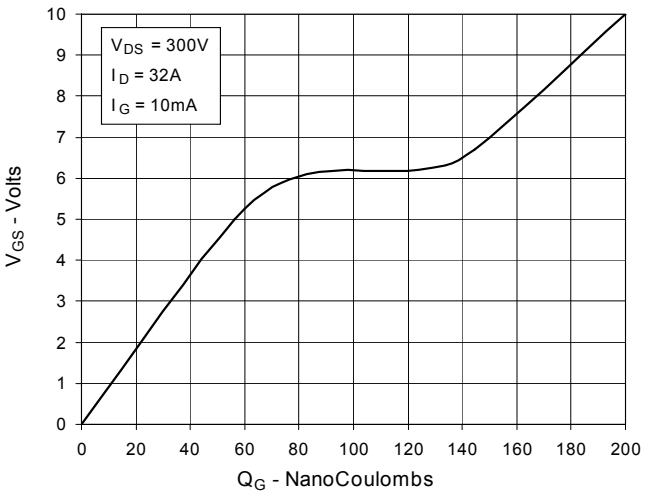


Fig. 11. Capacitance

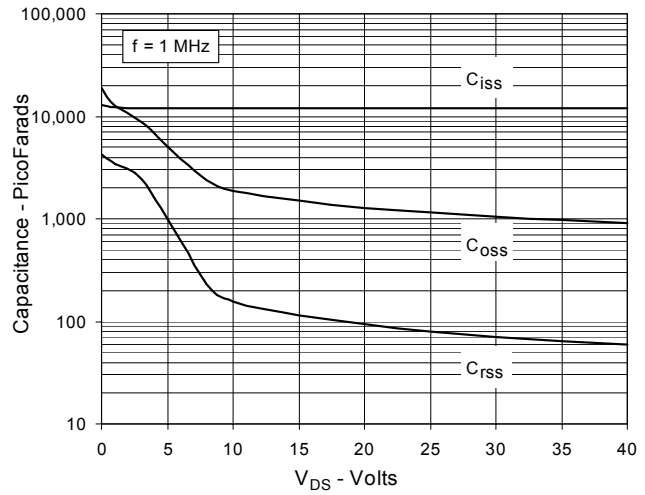


Fig. 12. Forward-Bias Safe Operating Area

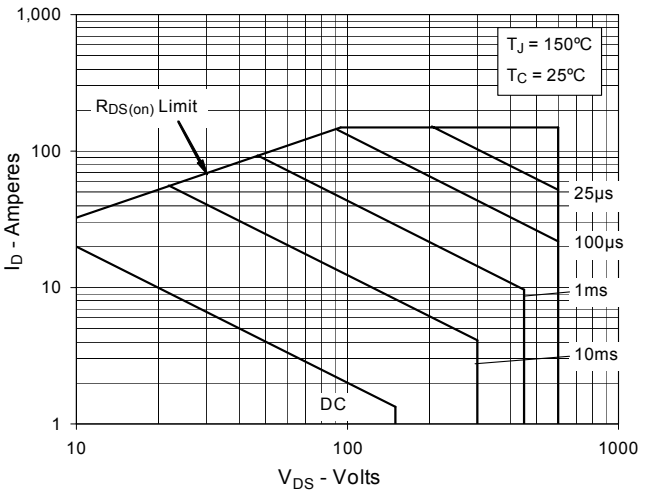


Fig. 13. Maximum Transient Thermal Resistance